Nicolet
NPC 800D

Nicolet

(415) 490-8300 TWX 910-381-7030

January 1, 1985

NPC-800D USER's:

Thank you for purchasing our NPC-800D Logic Analysis System.

We are currently completing the full-blown 800D Operator's Manual and the attached 11 page document is intended to serve as a temporary user's instruction until we can get the completed manual to you.

If you have any questions regarding the operation of the NPC-800D, please call our Logic Analysis Hotline:

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Our Applications Engineers will be happy to help you.

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An Introduction to Nicolet Paratronics Model 800D State Analyzer

1.0 BACKGROUND

This publication provides overview information for the Model 800D. A fully documented manual, containing various search and compare menus, is in the development stage and will soon be released.

1.1 Getting Started

Viewed from the front, the NPC*-800D Logic Analyzer features a fold-down ASCII keyboard with a row of six, special-purpose keys located directly beneath the CRT screen.

1.2 Use of Special-Purpose Keys

Special purpose keys help define and select data acquisition menus's and test parameters. To learn the keyboard, simply follow CRT prompts; special skills are not required.

1.3 Power-up

After using switch located on rear, right-side of the Model 800D to power on the system, allow sufficient time for CRT to warm up. When ready, a menu will appear.

1.4 Operational Menu - Top Line

The top line of this operational configuration menu displays the model number and software revision level.

1.5 Selection of Operational Mode

To select Operational mode, move inverse video block cursor up or down (using F4 or F5 keys) to the appropriate selection. This document discusses only the state menu (timing and other test and measurement items are covered in the operator's manual).

1.6 Collection

To perform a collection, simply depress F6 key (COLLECT). When memory is full and the collected data are displayed, the "labels" key directs you into the appropriate menu field that is required to alter the default conditions preprogrammed at the factory. As an alternative to pressing softkey F6, enter menu using F1 key, as directed by lower CRT display line. You may then setup triggering, clocking, or display conditions.

* Nicolet Paratronics Corporation

1.7 Cursor Movement

Once in the menu, by repeatedly pressing F2 (NEXT) or F1 (PREVIOUS) keys, you can move from one programmable field (indicated by reverse, half-lit video) to another. When block cursor is on desired field, movement within menu fields is accomplished with the space bar or backspace keys.

2.0 STATE SETUP MENU

The State Setup menu describes the Model 800D user display format, clocking scheme and event definitions (see Figure 1).

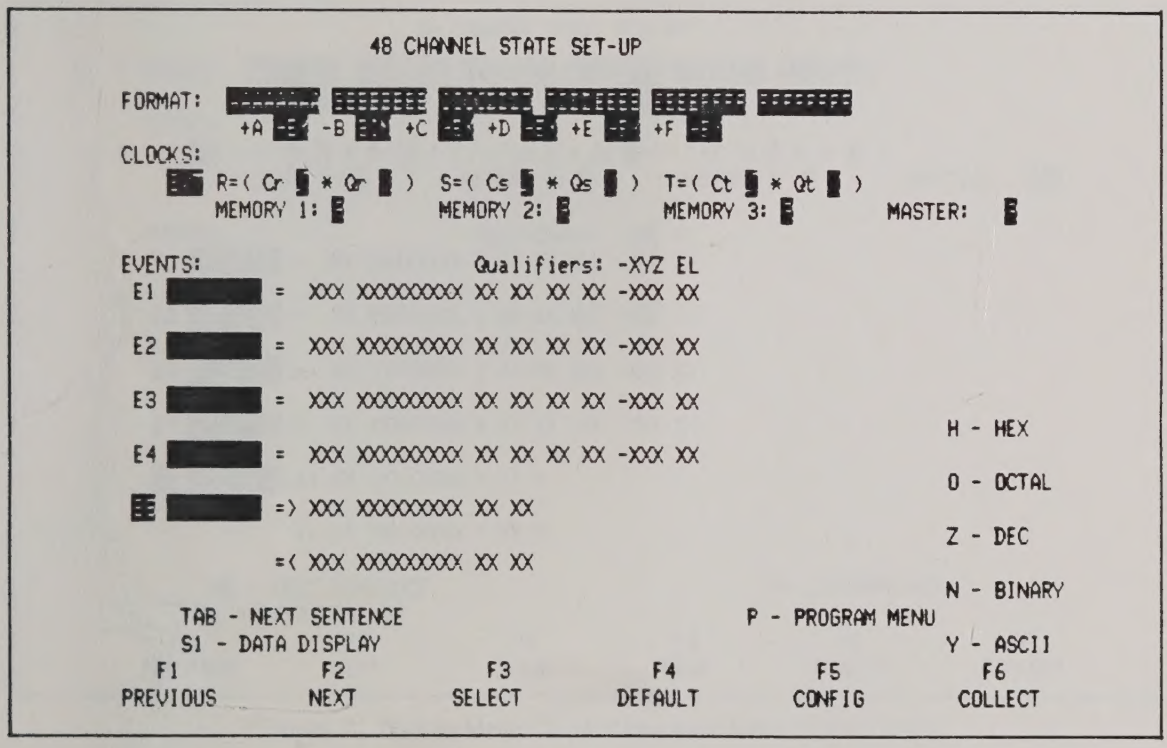

48 CHANNEL STATE SET-UP
FORMAT:
+A -B +C +D +E +F
CLOCKS:
R=(Cr * Qr) S=(Cs * Qs) T=(Ct * Qt)
MEMORY 1: MEMORY 2: MEMORY 3: MASTER:
EVENTS:
Qualifiers: -XYZ EL
E1 = XXX XXXXXXXX XX XX XX XX -XXX XX
E2 = XXX XXXXXXXX XX XX XX XX -XXX XX
E3 = XXX XXXXXXXX XX XX XX XX -XXX XX
E4 = XXX XXXXXXXX XX XX XX XX -XXX XX
=> XXX XXXXXXXX XX XX
=(XXX XXXXXXXX XX XX
H - HEX
O - OCTAL
Z - DEC
N - BINARY
Y - ASCII
TAB - NEXT SENTENCE
S1 - DATA DISPLAY
P - PROGRAM MENU
F1 PREVIOUS
F2 NEXT
F3 SELECT
F4 DEFAULT
F5 CONFIG
F6 COLLECT

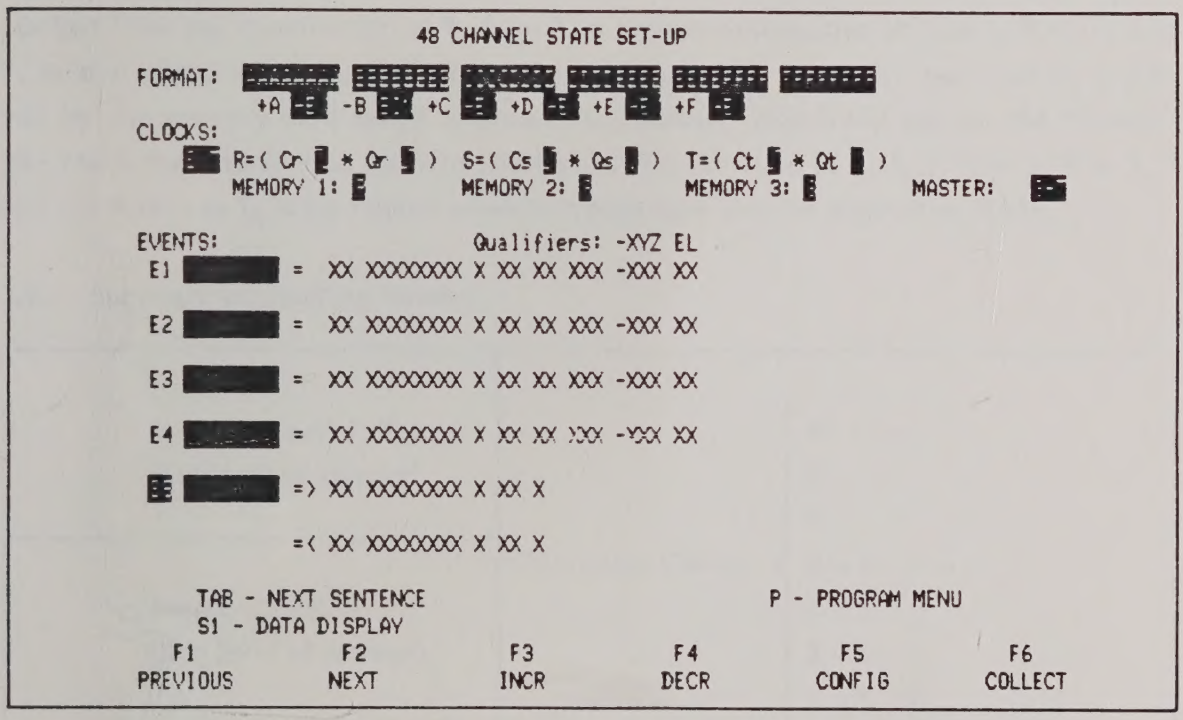
Figure 1. NPC Model 800D 48-Channel State Setup Menu

2.1 User-Defined Display Format

In the user-display format, you can select arbitrary labels (called A, B, C, D, E, and F) to define the number base of the grouping. Label names have no relationship to state probes names, yet define unbounded fields as inverted or noninverted when prefixed by - or + respectively (use F3 key to select polarity). As an example, the "binary" for B is inverted. Therefore, if data are turned right-side up in software, but you are interfacing the NPC analyzer to hardware, the display is still correct (see Figure 1).

2.2 Clocking Scheme

The NPC Model 800D has three clocks: R, S, and T (one for each probe). The R clock, which is defined as being equal to the clock logically AND'ed with the qualifier, can have edge or level or don't care qualifications (see Figure 2). When you logically AND two edges, it is interpreted as follows: a qualifying edge has to occur before a particular active clock edge. If there are repeated active clock edges before the qualifier, they are all ignored until the "qualifying" edge has occurred. The S and T clock also have a qualifier logically AND'ed with the clock. However, these two qualifiers can only be set as a 1, 0, or a don't care.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CLOCKS:
R=(Cr * Qr) S=(Cs * Qs) T=(Ct * Qt)
MEMORY 1: MEMORY 2: MEMORY 3: MASTER:
EVENTS: Qualifiers: -XYZ EL
E1 = XX XXXXXXXX X XX XX XXX -XXX XX
E2 = XX XXXXXXXX X XX XX XXX -XXX XX
E3 = XX XXXXXXXX X XX XX XXX -XXX XX
E4 = XX XXXXXXXX X XX XX XXX -XXX XX
=> XX XXXXXXXX X XX X
=(XX XXXXXXXX X XX X
TAB - NEXT SENTENCE
S1 - DATA DISPLAY
P - PROGRAM MENU
F1 PREVIOUS
F2 NEXT
F3 INCR
F4 DECR
F5 CONFIG
F6 COLLECT

Figure 2. Setup Menu With Edge and Level Qualifiers

By using extremely sophisticated triggering, an internal clock, (which can be selected with a repetition rate from 50 nanoseconds per sample to 50 milliseconds per sample), provides asynchronous collections up to 20 megahertz.

Data display is in tabular form only. For conversion of 16-channel (probe width) groupings into a timing diagram format, contact the NPC factory. Details are available for a program to perform such conversions.

NOTE

The state menu's internal asynchronous clock automatically uses the same clock as defined in the timing menu's clock. If the user is performing a cross-domain measurement, using both the state and timing analyzer sections of the Model 800D, this restriction may require a compromise clock selection.

Each 16-channel memory card (sufficiently wide for a one probe data connection) can be clocked from any combination of R, S, or T, a logical combination of R or S, R or T, S or T, or the logical combination of R or S or T, altogether. There are two clocking levels: one for the memory card (as an intermediate "holding" clock) and one for the "master" (the clock that stores data for later display). A combination of R, S, T, R or S, R or T, S or T, or R or S or T, is the master clock that puts data into the acquisition RAM.

2.2.1 Summary of Clocking Scheme

Memory Card: 1, 2, or 3 (1st level of storage)	Allowable Clocks: R, S, T, R + S, R + T, S + T, R + S + T
Master Clock (2nd level of storage)	

By using these clock fields, virtually any microprocessor, multiplexing, or clocking scheme can be accommodated with the Model 800D. Clocks R, S, and T can now handle multiple frequencies, not just multiple phases (as in all of NPC's preceding state analyzers). If you are at different frequencies, phase has no meaning. For example, a 2-MHz phase is not relative to a 3-MHz phase because they are at different frequencies. To make them relative, all phase measurements need a base starting point.

2.3. Dedicated Microprocessor Personality Probes

On probes that have rotary selector switches, qualifiers are used as follows: Q_R and Q_S (Q_T is not used) are clock qualifiers connected into the rotary knobs. The following table

illustrates the use of the polarity (sense) clock qualifier (on the Model 800D) with the dedicated personality pod rotary knob settings:

Q_R, Q_S, { 0 = qualifies on knob position; X = ignores knob setting; 1 = disqualifies on knob position; Q_T is not used on NPC's probes. } where $Q_R = A_2$ knob; where $Q_S = A_1$ knob

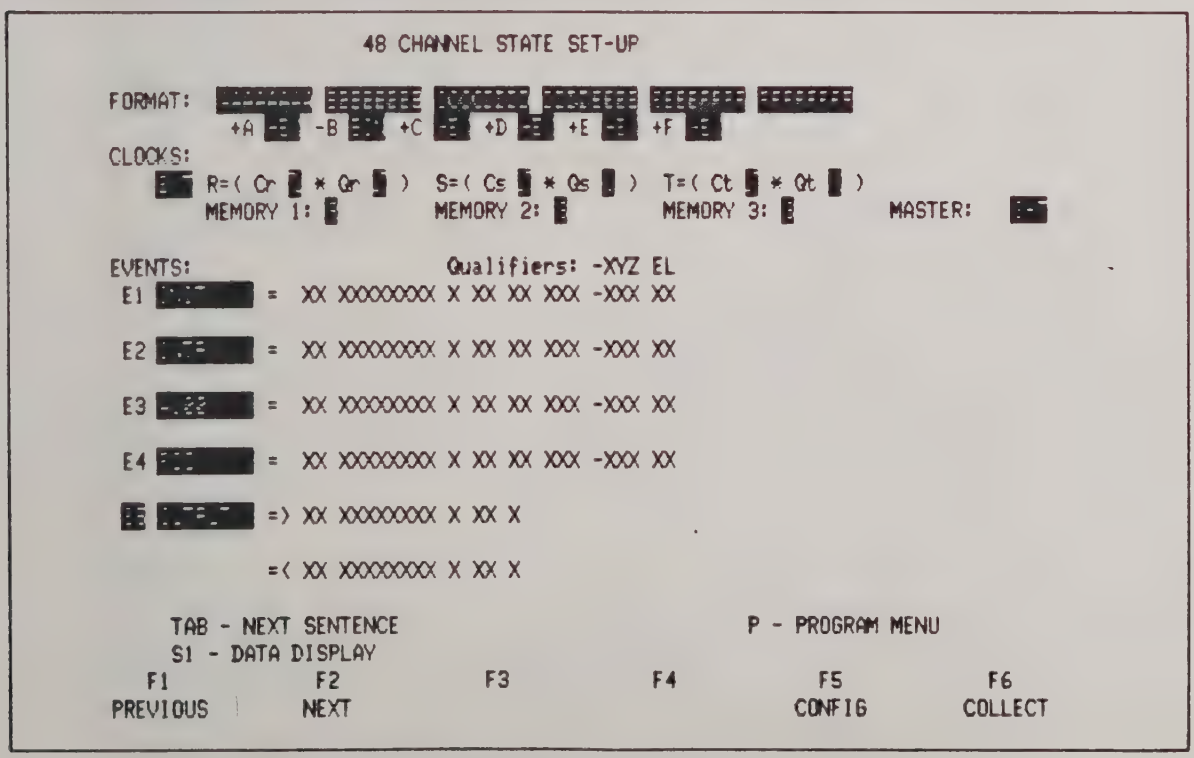
XYZ qualifiers, which are separate, are used to further restrict an event definition from some target hardware lines (connected to them). Event qualifiers X, Y, and Z are programmed to adhere to the following table:

X, Y, and Z { 1 qualifies; X ignores; 0 disqualifies } where X = A_1; where Y = A_2

For better flexibility, $Q_{R,S,T}$ clock qualifier input lines do not "eat up" word recognizers.

2.4 Event Definition

Event Definition is the third item of the state set-up menu. In the Model 800D, you can choose from four event and one range or from five event comparators. They can be defined symbolically to have "tie-ins" with the user's software (see Figure 3). For example, E1 is INIT, E2 is INTR, E3 is A100, E4 is FOO, and Range 1 is an OUTPUT.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E2 = XX XXXXXXXX X XX XX XXX -XXX XX
E3 = XX XXXXXXXX X XX XX XXX -XXX XX
E4 = XX XXXXXXXX X XX XX XXX -XXX XX
=) XX XXXXXXXX X XX X
=(XX XXXXXXXX X XX X
TAB - NEXT SENTENCE
S1 - DATA DISPLAY
P - PROGRAM MENU
F1 PREVIOUS
F2 NEXT
F3
F4
F5 CONFIG
F6 COLLECT

Figure 3. Setup Menu With Events/Range Defined

An event, which is logically defined in terms of the user-defined format field, can be setup in whatever number base(s) that has been selected. A qualifier is on the right-hand side of each event, after the hyphen. There is an X, Y, Z, E, and L qualifier. X, Y and Z refer to the three external hardware qualifier line inputs for this state memory card. These inputs are not displayed with data, but help restrict the collection. They perform the same function as the AA, BB, CC qualifiers displayed on previous state analyzers manufactured by NPC. E is the external input from the BNC (on rear apron), and L is the link bit from the timing analyzer. Range definition is greater than or equal to a lower limit and less than or equal to an upper limit. Each limit is 32-bits wide. This 32-bit range is very powerful; it allows, for example, the definition of a range within or outside of a window of addresses to be collected (see Figure 4).

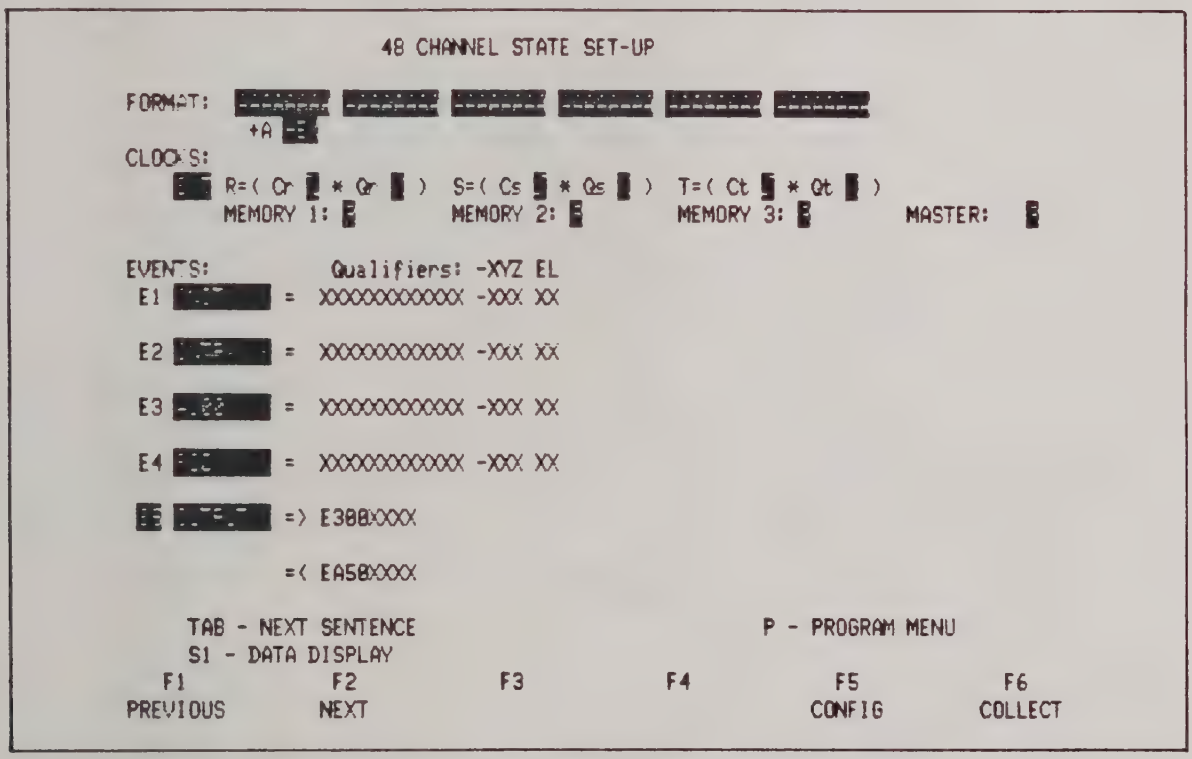


Figure 4. Event Definition Using a Range of Values

This summarizes the state setup menu. When ready to program, the state analyzer displays (in lower right corner) P-PROGRAM MENU. When you press this key, (P), you enter the program menu.

3.0 STATE PROGRAM MENU

The top line of the Model NPC-800D 48-channel state program menu transfers symbolic event definitions from the state setup menu (see Figure 5).

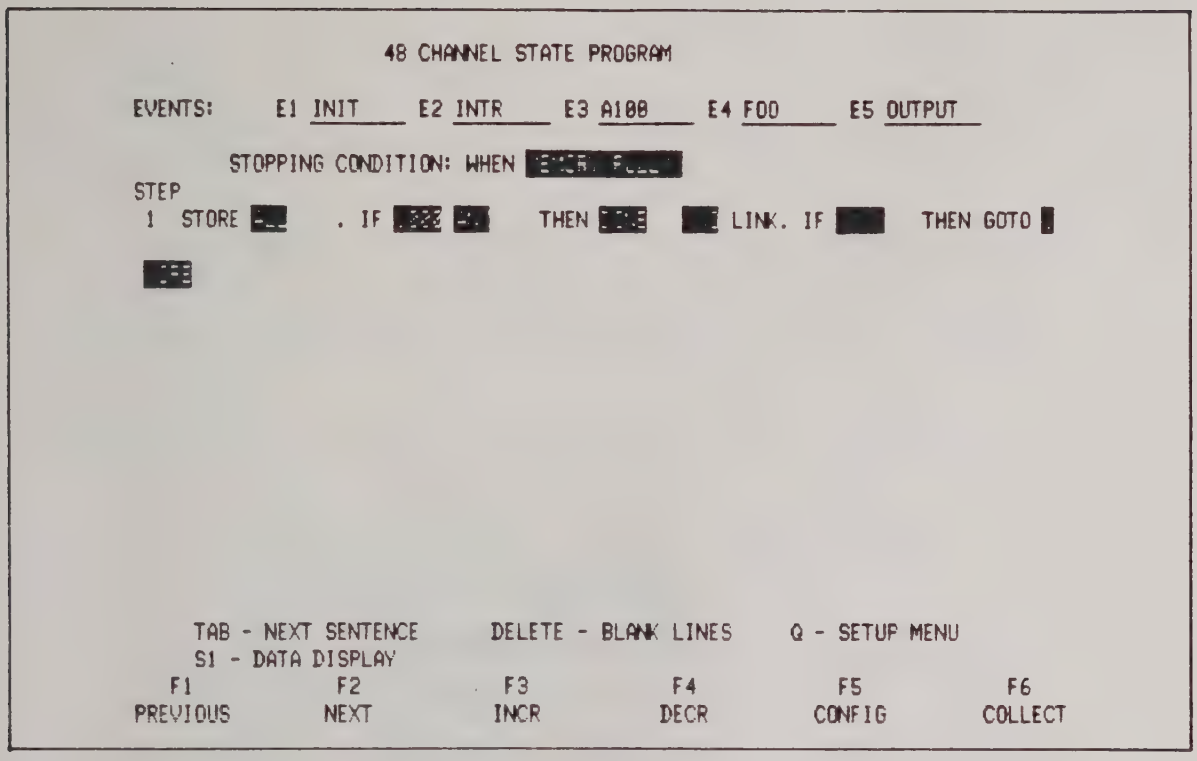


Figure 5. State Program Menu (With Transferred Event Names)

3.1 Quick Summary

Stopping conditions for the analyzer's data acquisition can be either "when the sequence is done" (sequence of steps defined below) or "when acquisition memory is full." There is a maximum of eight steps; each step is divided into three sentences: a store sentence, the first "IF" condition, and a second "IF" condition.

3.2 Three Sentences

Using the store sentence, you can store an event, the logical 'OR' combination of an event, or not an event; store everything, or store nothing. The first "IF" condition refers to events from the set-up menu. For example, on step number one, if 1000 of event E1 occur (those INIT events) then go on to step number two. Do not perform any linking. Also, on step one, the second "IF" condition will say "If you're not done, then go on back to step number one and continue until you do have 1000 E1's before moving on." The first "IF" condition has a pass counter with which you can count clocks or events (similar to delayed modes found in previous NPC state models). The second "IF" condition, which is simpler, has no counter. The first "IF" condition also harnesses linking capabilities. At any step of the sequence, you may or may not provide a link. As in previous state analyzer models from NPC, it is no longer "latched-on" until the memory is filled.

3.3 Priority Of First "IF" And Delays

If, for some reason, both "IF" conditions are programmed with exactly the same situation, the first sentence (with counter in it) takes priority.

If, as in step 3 of Figure 6, there are 500 of "any", this means there are 500 master clocks, (that is, 500 clocking events have been completed). Therefore, you can delay by events (as in step numbers 1 and 2), or you can delay by master clocks, in step number 3.

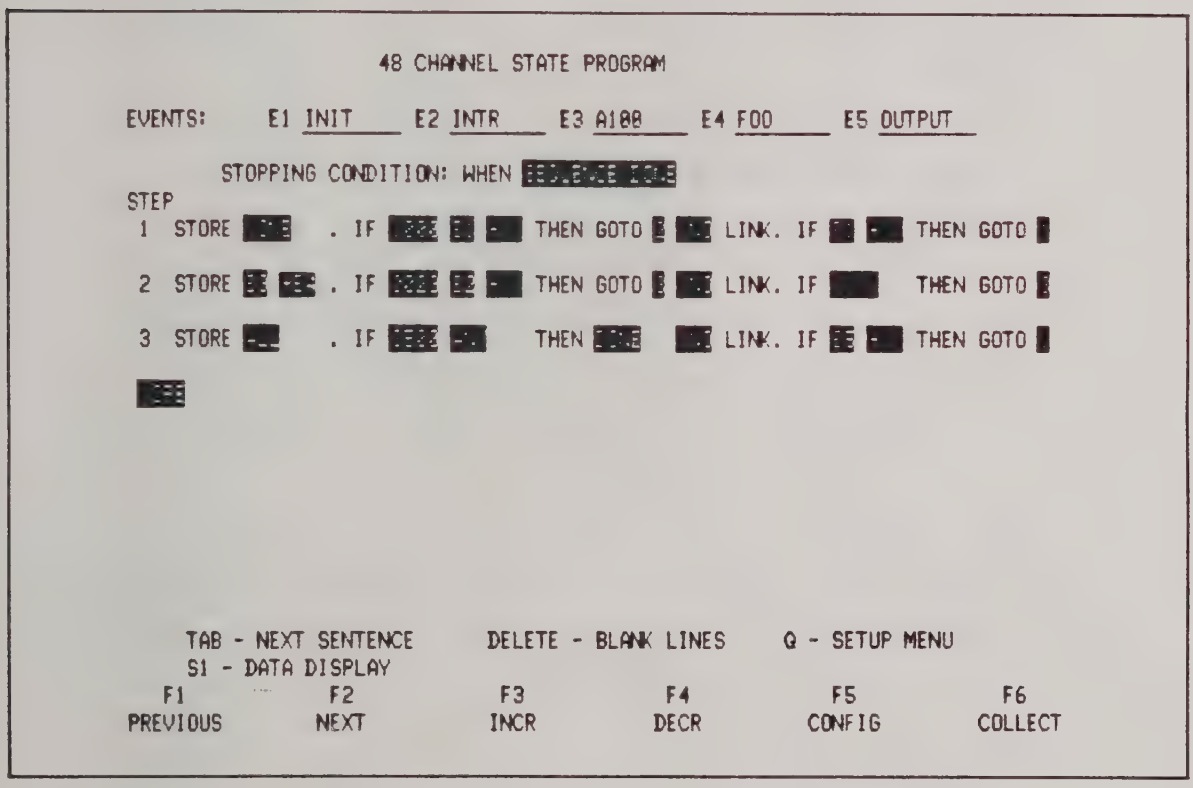

48 CHANNEL STATE PROGRAM
EVENTS: E1 INIT E2 INTR E3 A100 E4 F00 E5 OUTPUT
STOPPING CONDITION: WHEN
STEP
1 STORE . IF THEN GOTO LINK. IF THEN GOTO
2 STORE . IF THEN GOTO LINK. IF THEN GOTO
3 STORE . IF THEN LINK. IF THEN GOTO
TAB - NEXT SENTENCE
DELETE - BLANK LINES
Q - SETUP MENU
S1 - DATA DISPLAY
F1 PREVIOUS
F2 NEXT
F3 INCR
F4 DECR
F5 CONFIG
F6 COLLECT

Figure 6. Three Program Steps Illustrating Clock/Event Delay

3.4 Criss-Crossing In The Menu

You can specify up to eight steps. One step can jump up or down (that is, from step one down to step five and then back up to step three and then up to step two); it is virtually possible to move anywhere in this eight step sequence (see Figure 7).

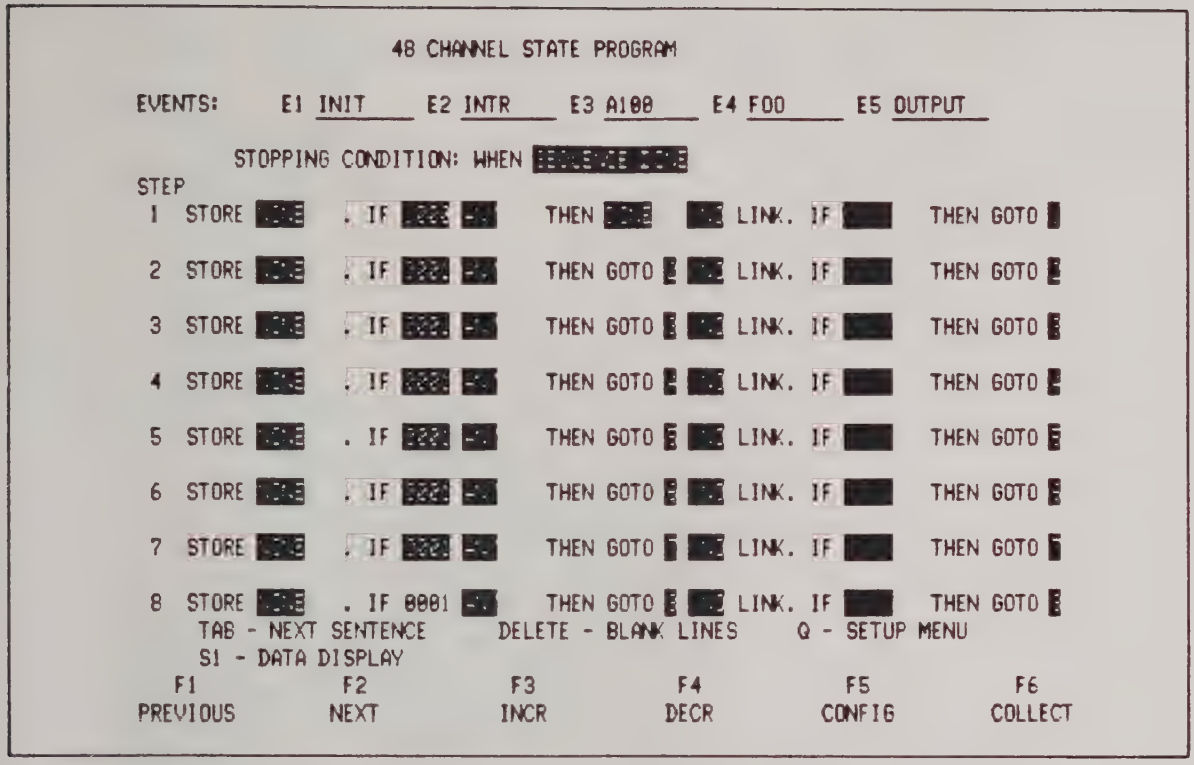

48 CHANNEL STATE PROGRAM
EVENTS: E1 INIT E2 INTR E3 A100 E4 F00 E5 OUTPUT
STOPPING CONDITION: WHEN
STEP
1 STORE . IF THEN LINK. IF THEN GOTO
2 STORE . IF THEN GOTO LINK. IF THEN GOTO
3 STORE . IF THEN GOTO LINK. IF THEN GOTO
4 STORE . IF THEN GOTO LINK. IF THEN GOTO
5 STORE . IF THEN GOTO LINK. IF THEN GOTO
6 STORE . IF THEN GOTO LINK. IF THEN GOTO
7 STORE . IF THEN GOTO LINK. IF THEN GOTO
8 STORE . IF 0001 THEN GOTO LINK. IF THEN GOTO
TAB - NEXT SENTENCE DELETE - BLANK LINES Q - SETUP MENU
S1 - DATA DISPLAY
F1 PREVIOUS
F2 NEXT
F3 INCR
F4 DECR
F5 CONFIG
F6 COLLECT

Figure 7. Setup Menu With An Eight-Step Sequence

"Triggering" takes on new significance in the Model 800D state analyzer. In previous NPC models, triggering was defined as "the starting or stopping process of the logic analyzer." Now there is essentially "no" triggering (as such) except when the memory is full or when the sequence is complete. Because this is an "event"-oriented machine, you specify, using the store field, what must be recorded.

4.0 SEARCH AND COMPARE MENUS

This menu consists of two parts: one part searches for a condition in an existing data collection already residing in main memory; the other part searches to "dynamically compare" a reference data block with the recently acquired data block in the main memory (see Figure 8).

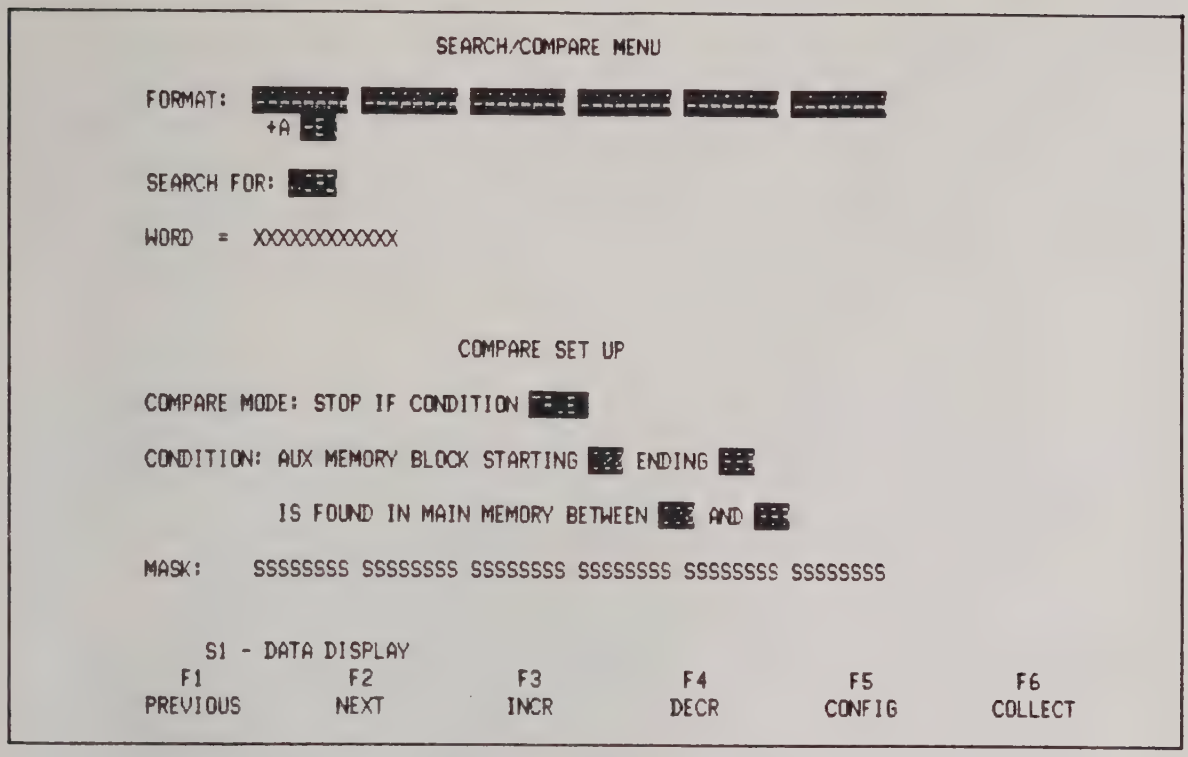


Figure 8. Search and Compare Menu With Default Conditions

The top line is the user format, carried over from the Setup menu (where it is created or altered). Because it is not an inverse video half-lit field, it is not programmable from this menu.

The user can search for the following in either the main or the auxiliary memory:

1. a word (up to 48-display-bits wide) or **not** a specific word,
2. a range (with upper or lower bounds) or **not** a range (equivalent to searching for something within or outside of a window), and
3. an event (symbollically labeled from the Setup menu) or **not** that event.

The compare setup allows the user to compare dynamically (with or without equality) to a reference collection residing in the auxiliary memory.

4.1.1 Stopping Conditions

If the reference is the same as the main state memory or if it is different than the main state memory, the stopping condition can be set to hold (stops subsequent comparisons). This can be called "hold if equal to" or "hold if not equal to," respectively. If it is equal, the stopping condition is true; if false, then it holds when a difference occurs.

4.1.2. Area Comparisons

The entire main memory can be compared to the entire auxiliary memory or a small subset of each could be compared to a different subset of the other. For example, even if there is a displacement between locations from the trigger point, a block of 50 words could be compared in the auxiliary memory to a block of 100 words in the main memory.

4.1.3 Example

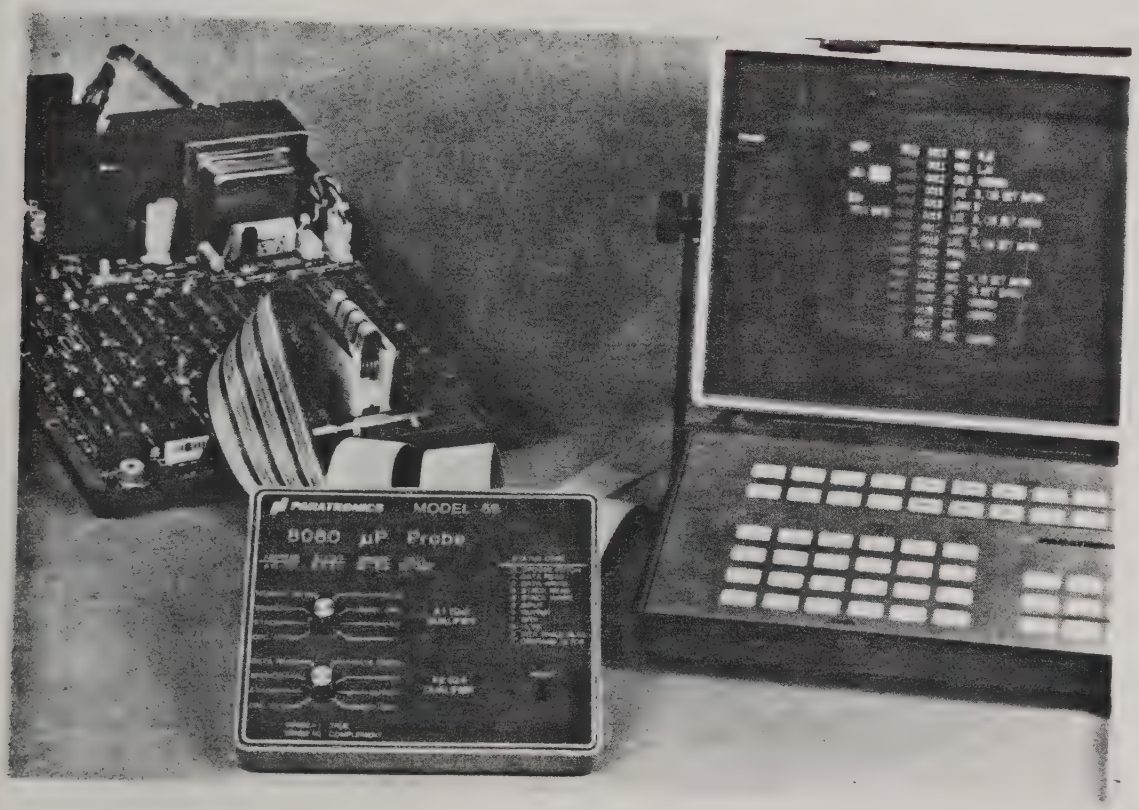
For a subset comparison, an example is required. If locations 250 to 254 in auxiliary memory are to be compared to locations 000 to 500 in main memory, the following occurs: if "true stopping collection" is selected, five locations in auxiliary memory will (when found in sequence in first 500 locations in main memory) stop the collection process.

4.1.4 The Mask

To speed up the comparison process, only a section of the total 48-channel width of the state machine needs to be compared. A "don't-care" (X) can be placed anywhere in the mask to identify channels not to participate in the comparison process.

USER'S INSTRUCTIONS

ANALYSIS OF THE 8085 MICROPROCESSOR USING THE PI-540/PI-648/NPC-748 OR NPC-764 LOGIC ANALYSIS SYSTEM AND THE MODEL 56 DEDICATED PROBE



Typical Dedicated Probe Set-up.
(The Model 56 probe is virtually identical to the Model 55 probe shown here.)

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150-8085-0001C

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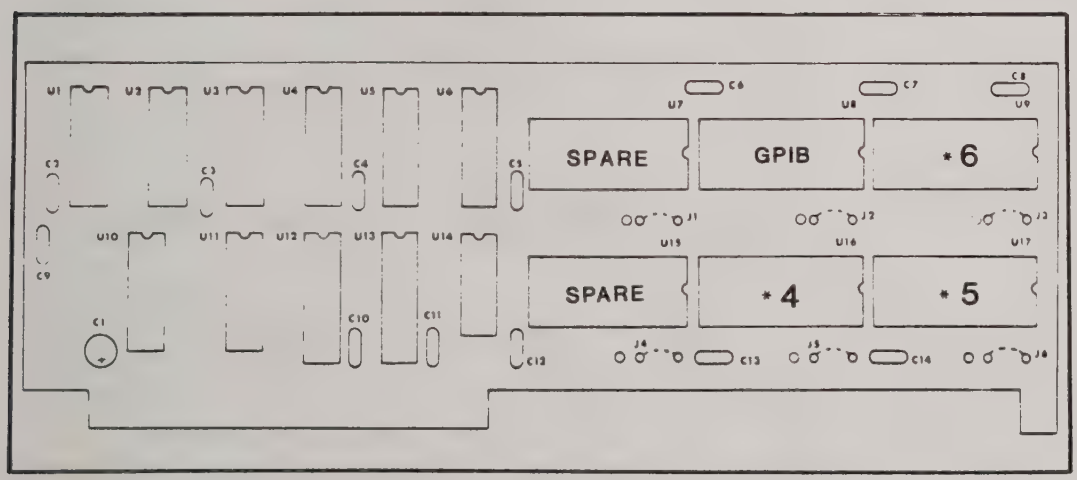
INTRODUCTION

The purpose of this user's instruction is to show the 8085 user how to take advantage of the powerful analysis capabilities of the Nicolet Paratronics' PI-540, PI-648, NPC-748 and NPC-764 family of Logic Analyzers used with a Model 56 dedicated probe. References to the term "Analyzer" means that the information applies to either the PI-540, PI-648, NPC-748 or NPC-764. (They are completely interchangeable when each is equipped with the associated disassembler software.)

The Model 56 offers quick, convenient, connection to the microprocessor-under-test because it is terminated with a pre-wired 40-pin DIP clip. The necessary signals for clocking data into the Analyzer are automatically generated by the probe. Note that the 8085 data collection can include 16 address lines, 8 data lines, 4 cycle status lines, and 2 user-defined signals.

The probe utilizes the unique clock and trigger qualifiers of the Analyzer to simplify the analysis of program execution. You can select these clock or trigger qualifiers, or combinations of both, to capture only the categories of program flow required to solve a particular problem.

For the PI-540, PI-648, and NPC-748 the disassembly software resides in PROM (Figure 1-1). If the disassembly software (a single PROM) is installed, the Analyzer will "comment" each line of recorded data with specific cycle status information such as MEM READ, MEM WRITE, ADD, LD, I/O, OPERAND FETCH, etc. To activate the disassembly, press the *4 key in the Analyzer's DISPLAY grouping for the PI-540, *1 for the PI-648. For the NPC-748, simply press the "1" key.



gure 1-1. **Location of disassembly PROMs on extended memory board corresponding to *4, *5, and *6 keys on the PI-540. Note that the analyzer's mainline software changes to accommodate the various disassembly locations. The PI-648 and NPC-748 do not require extended memory boards. The disassembly PROMs are located at slot U15 of the processor board for these systems.**

The NPC-764 disassembly software resides on the diskette, with activation being accomplished by the following keystrokes:

- Escaping to the disk operating system by depressing ESC
- After the A> prompt type LADISA DZ80 and return
- Depressing the F1 soft function key and viewing the acquired data
- Activating the disassembler with the I key

NOTE: With the NPC-764 other number bases are still accessible as before via the LABELS key menu.

2.0 INITIAL SET-UP

2.1 Connect the Model 56's blue ribbon cables to the Analyzer as follows:

a. Left cable goes to STATE A CHNL.

b. Right cable goes to STATE B CHNL.

NOTE: 1. The Model 56's cables are conveniently labeled "THIS SIDE UP."

2. Before continuing, make certain that the system-under-test (SUT) is powered down.

2.2 Connect the Model 56's 40-pin DIP clip to the 8085 under test, making certain that the keyed pin of the clip is connected to Pin 1 of the microprocessor.

2.3 Set switches A1 and A2 on the Model 56 to the OPC FETCH position. See Figure 2-1.

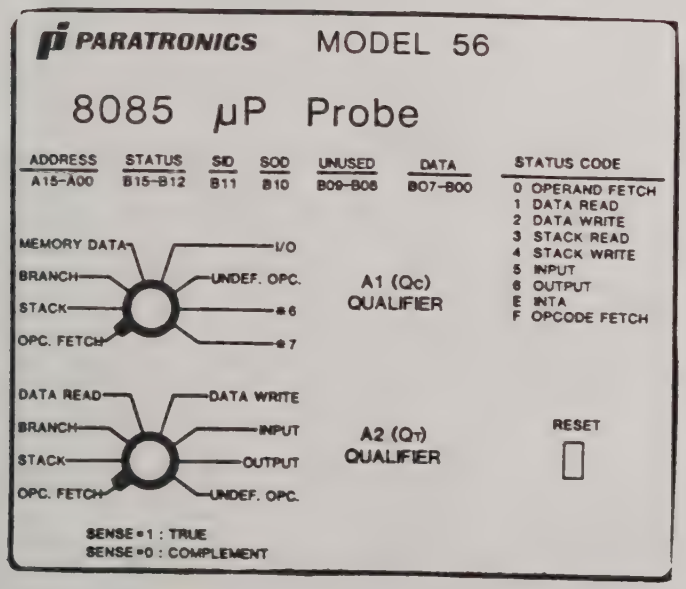


Figure 2-1. Model 56 Front Panel.

2.4 Power on the Analyzer and wait for the CONFIGURATION LIST to appear. Select the 32 CHNL STATE mode for the PI-540 and the NPC-748, or the 48 CHNL STATE mode for the PI-648 and NPC-764. Then access the associated state menu.

2.5 Set the menu parameters to match those in Figure 2-2. It is suggested that the Display Format in this figure be made to agree with the format information on the Model 56 probe for the purpose of clarity in this application note. However, you'll find that the format can be varied according to your specific application without affecting the disassembly function.

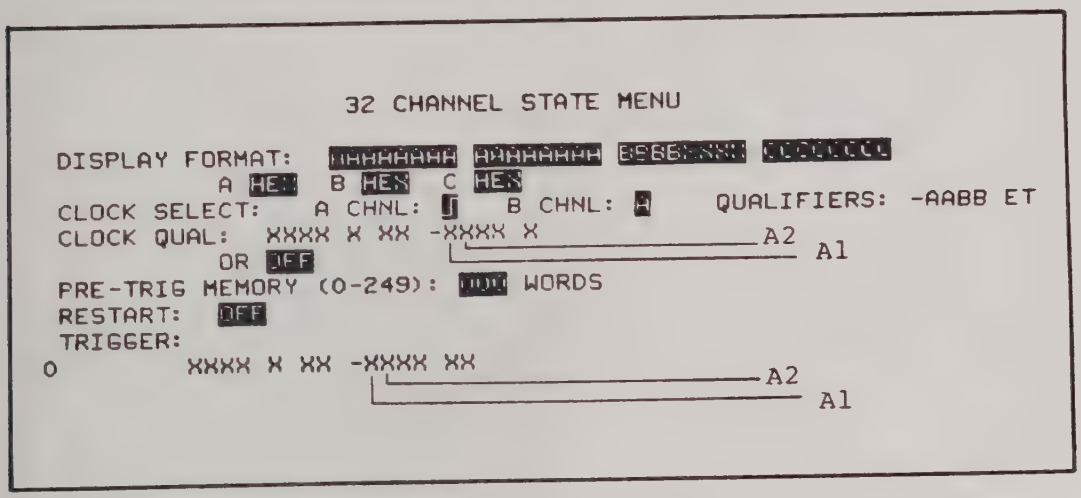


Figure 2-2. 32 Channel State Menu.
A1 and A2 set to binary 1 (or ∅) to enable corresponding qualifier.
(Note: 48 channel on PI-648 and NPC-764 is similar)

3.0 CLOCK AND TRIGGER QUALIFYING

The Model 56 probe utilizes two of the Analyzer's menu-selectable qualifiers, as shown in Figure 2-2. In this figure, the applicable qualifier bits are called A1 and A2. Depending upon the field they are used in, A1 and A2 can represent clock qualifiers or trigger qualifiers. Or, one can be used in the clock qualifier field while the other is used in the trigger qualifier field. (Note that **clock** qualification is used to collect certain types or categories of bus transactions such as memory or I/O operations; while **trigger** qualification is used to "arm" the analyzer for triggering when a pre-specified memory, I/O, or other event occurs.) Refer to the Clocks and Qualifiers section of the Analyzer Operator's Manual for additional information.

3.1 CLOCK Qualification (A1 or A2 or Both)

The clock qualifier restricts collected data to certain types of operations, such as OPCODE FETCHES, I/O OPERATIONS, BRANCHES, STACKS, etc. With this ability to select a specific operation, you can maximize the utilization of the Analyzer's memory. Note that the Analyzer/Model 56 combination can also be

used to eliminate a specific type of operation. For example, you can set qualifiers A1 or A2 in the Analyzer state menu to a "0" and the corresponding function switch on the Model 56 to BRANCH so that all BRANCH operations are eliminated (or excluded) from the data collection. See Tables 3-1(a) and 3-1(b) for a listing of the various **clock** qualification functions using A1 and A2.

.2 TRIGGER Qualification (A1 or A2 or Both)

The qualifiers (A1, A2) can be used to link the trigger word to the occurrence of other events. For example, A1 or A2 can be set to a BRANCH signal used with the address and/or data information enabling you to locate a problem in a particular subroutine. See Tables 3-2(a) and 3-2(b) for a listing of the various **trigger** qualification functions using A1 and A2.

Table 3-1(a). Clock Qualification Using A1.

MODEL 56 .1 Qualifier Switch	State Analyzer Clock Qualifier Field With A1 = 1	State Analyzer Clock Qualifier Field With A1 = 0
)PCODE FETCH	Collects only program information, for applications where data are not required.	Collects all operations **except** OPCODE FETCHES.
TACK	Collects only stack information. Particularly useful in stack overflow problems.	Collects all operations **except** STACK.
RANCH	Collects only BRANCH information to monitor changes in program flow for extended "control" tracing.	Collects all operations **except** STACK.
6, *7	Collect data only when the associated user-defined signal is **high.**	Collect data only when a user-defined signal is **low.**
IEMORY DATA	Collect only memory data read/write operations. (Usually used with a specified address.)	Exclude memory data read/write operations from data collection.
O	Collect only Input and Output operations. May be used with specified port address.	Exclude I/O operations from data collection.

Table 3-1(b). Clock Qualification Using A2.

MODEL 56 .1 Qualifier Switch	State Analyzer Trigger Qualifier Field With A2 = 1	State Analyzer Trigger Qualifier Field With A2 = 0
)PCODE FETCH	Collects only program information for applications where data are not required.	Collects all operations **except** OPCODE FETCHES.
TACK	Collects only stack information. Particularly useful in stack overflow problems.	Collects all operations **except** STACK.
BRANCH	Collects only BRANCH information to monitor changes in program flow for extended "control" tracing.	Collects all operations **except** STACK.
)ATA READ/)ATA WRITE	Collects only DATA READ/ WRITE operations (as distinguished from OPERAND FETCHES and STACK OPS).	Collect all operations **except** DATA READ/ DATA WRITE.
NPUT/OUTPUT	Collect only INPUT/OUTPUT cycles.	Collect all operations **except** INPUT/OUTPUT.
JNDEFINED)PCODES	Collect only UNDEFINED OPCODES. (CPU is "lost.")	Not applicable.

NOTE: In Tables 3-1(a) and (b), A1 and A2 can both be used for clock qualification.

Table 3-2(a). Trigger Qualification Using A1.

MODEL 56 A1 Qualifier Switch	State Analyzer Trigger Qualifier Field With A1 = 1	State Analyzer Trigger Qualifier Field With A1 = 0
OPCODE FETCH	Trigger when a particular address is accessed for an OPCODE FETCH only.	Trigger on anything **except** OPCODE FETCH.
STACK	Used with specific address. Trigger when stack reaches a certain (overflow) depth.	Trigger on anything **except** STACK.
BRANCH	Similar to OPCODE FETCH.	Trigger on anything **except** BRANCH.
MEMORY DATA	Trigger on memory data read **or** write. (Usually used with a specified address.)	Trigger on anything **other than** memory data read or write (from specified address, if any).
I/O	Trigger on an input or output operation. (Usually from a specified port address.)	Trigger on anything **other than** an input or output operation.
*6, *7	Trigger on the associated user-specified signal if it is **high.**	Trigger on a user-specified signal if it is **low.**

Table 3-2(b). Trigger Qualification Using A2.

MODEL 56 A2 Qualifier Switch	State Analyzer Trigger Qualifier Field With A2 = 1	State Analyzer Trigger Qualifier Field With A2 = 0
OPCODE FETCH	Trigger when a particular (if any) address is accessed for an OPCODE FETCH only.	Trigger on anything **except** OPCODE FETCH.
STACK	Used with specific address. Trigger when stack reaches a certain (overflow) depth.	Trigger on anything **except** STACK.
BRANCH	Similar to OPCODE FETCH.	Trigger on anything **except** BRANCH.
DATA READ/ DATA WRITE	Trigger on DATA READ/WRITE from specific address, if any.	Trigger on anything **except** DATA READ/ DATA WRITE.
INPUT/OUTPUT	Trigger on an INPUT/OUTPUT operation from the associated user-specified port.	Trigger on anything **except** INPUT/ OUTPUT.
UNDEFINED OPCODES	Trigger on the occurrence of an undefined opcode. (CPU is "lost".)	Not applicable.

NOTE: In Tables 3-2(a) and (b), A1 and A2 can both be used for trigger qualification.

OPERATION

The following examples demonstrate the versatility of the Model 56 probe when combined with the disassembly software. The first example uses the basic menu shown in Figure 2-2. The remaining examples are more advanced. Note that the 4 user-defined status lines, B15-B12, are **not** part of these examples (See Figure 2-1).

Example 1. Collecting All Address and Data Transactions.

In this example, both A1 and A2 in the Analyzer clock and trigger qualifier fields were set to X's (don't care) so that **all** information on the address and data busses can be collected. The positions of the A1 and A2 switches on the Model 56 do not matter in this case. Note that for this example, the trigger word was chosen as address (0000) HEX. For your system, you may want to initially set the trigger word as all X's for a random data collection, which will verify that the set-up is functioning properly.

```
MAIN          TRIG  0000  IN   PORT:47
              +001  0011      47     OPERAND FETCH
LOC:  TRIG    +002  0003  LXI    SP,10FFH
              +003  0003      FF     OPERAND FETCH
SIG:  2E93    +004  0004      10     OPERAND FETCH
      1391    +00F  0005  LXI    H,1000H
      100F    +00E  0006      00     OPERAND FETCH
              +00D  0007      10     OPERAND FETCH
              +00B  0018  MVI    B,F0H
              +009  0009      F0     OPERAND FETCH
              +010  000A  MVI    M,00H
              +011  0003      00     OPERAND FETCH
              +012  000C  INX    H
              +013  0009  DCR    B
              +014  000C  JNZ    000A
              +015  000F      0A     OPERAND FETCH
```

Figure 4-1. General Data Collection.
(Your data may differ.)

NOTE: The PI-540's Binary, Octal, Decimal, and ASCII keys can be used to convert Hex address and data to other display formats; however, in the disassembly mode, address and data are displayed only in Hex. Also in the disassembly mode, the actual operands and destination addresses are displayed only if the respective data are collected, i.e., not purged by qualifier(s).

4.2 Example 2. Collecting OPCODE FETCHES using A1 as a Clock Qualifier.

To collect OPCODE FETCHES only, set up the Analyzer/Model 56 as follows:

PI-648 MENU* (Figure 4-2.1)	MODEL 56 SWITCHES (Figure 2-1)
Qualifier A1 = 1	Switch A1 = OPCODE FETCH
Qualifier A2 = X	Switch A2 = makes no difference

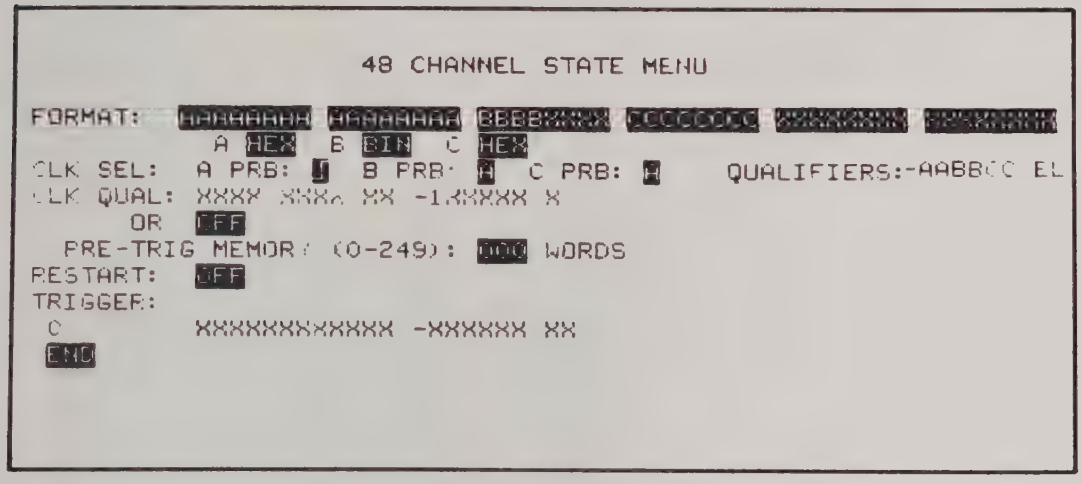


Figure 4-2.1. Menu Set-Up.

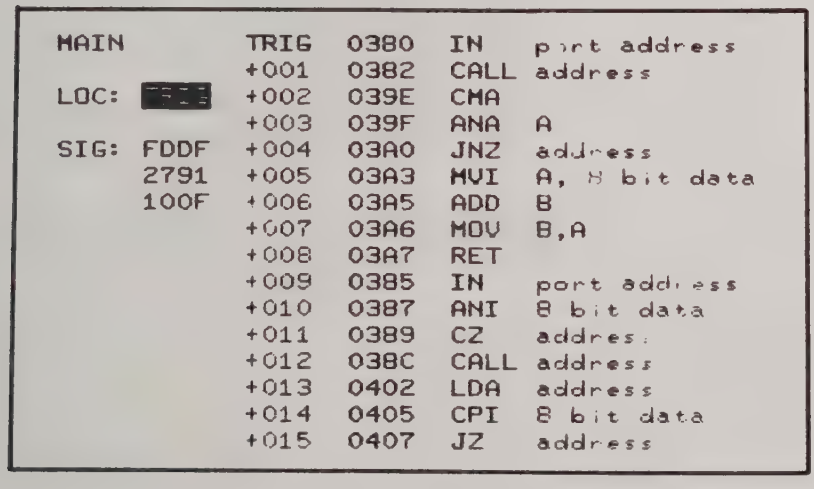

MAIN TRIG 0380 IN port address
+001 0382 CALL address
LOC:
+002 039E CMA
+003 039F ANA A
SIG: FDDF +004 03A0 JNZ address
2791 +005 03A3 MVI A, 8 bit data
100F +006 03A5 ADD B
+007 03A6 MOV B,A
+008 03A7 RET
+009 0385 IN port address
+010 0387 ANI 8 bit data
+011 0389 CZ address
+012 038C CALL address
+013 0402 LDA address
+014 0405 CPI 8 bit data
+015 0407 JZ address

Figure 4-2.2. Using A1 for Collecting OPCODE FETCHES Only. (Your data may differ.)

***The PI-540, NPC-748, and NPC-764 menus are similar.**

.3 Example 3. Collecting Stack Operations Using A1 as a Clock Qualifier.

To collect STACK operations only, set up the Analyzer/Model 56 as follows:

ANALYZER MENU (Figure 4-2.1)	MODEL 56 SWITCHES (Figure 2-1)
Qualifier A1 = 1	Switch A1 = STACK
Qualifier A2 = X	Switch A2 = makes no difference

```
MAIN          TRIG   10EF    67     STACK READ
              +001   10F0    03     STACK READ
LOC:  [    ]  +002   10F0    03     STACK WRITE
              +003   10EF    6C     STACK WRITE
SIG:  A80E    +004   10EF    6C     STACK READ
      8E0D    +005   10F0    03     STACK READ
      100F    +006   10F0    03     STACK WRITE
              +007   10EF    71     STACK WRITE
              +008   10EF    71     STACK READ
              +009   10F0    03     STACK READ
              +010   10F0    03     STACK WRITE
              +011   10EF    76     STACK WRITE
              +012   10EF    76     STACK READ
              +013   10F0    03     STACK READ
              +014   10F0    03     STACK WRITE
              +015   10EF    7B     STACK WRITE
```

Figure 4-3. Using A1 for Collecting Stack Operations Only. (Your data may differ.)

4.4 Example 4. Data Qualified Clocking (A1 and A2 are not used).

The collection of address and data information can be further qualified by utilizing the two OR'ed clock qualifiers in the Analyzer state menu. (See Figure 4-4.1.) With these qualifiers, it is possible to collect a selected range of addresses and data. In the menu in Figure 4-4.1, notice the CLOCK QUAL parameter. The first of two qualifiers for the first 16 bits of address information has been formatted in hex. This address word has been set to all zeros, except the two least significant bits which were set to "don't care's" (X). This set-up results in the logic analyzer collecting any addresses between 0000 (HEX) and 00FF (HEX). The second qualifier, which is OR'ed with the first, has been set to collect address DXXX (HEX).

```
                    32 CHANNEL STATE MENU

 DISPLAY FORMAT:  AAAAAAAA AAAAAAAA BBBBXXXX CCCCCCCC
          A HEX  B HEX  C HEX
 CLOCK SELECT:    A CHNL: 1    B CHNL: 4     QUALIFIERS: -AABB ET
 CLOCK QUAL:  00XX X XX -XXXX X
          OR DXXX X XX -XXXX X
 PRE-TRIG MEMORY (0-249): 000 WORDS
 RESTART:  OFF
 TRIGGER:
0         XXXXXXXX -XXXX XX
END
```

Figure 4-4.1. Sample Menu for Data Qualified Clocking With A1 and A2 Not Used (Your data may differ.)

STATE ANALYZER MENU (Figure 2-2)	MODEL 56 SWITCHES (Figure 2-1)
Qualifier A1 = X	Switch A1 = makes no difference
Qualifier A2 = X	Switch A2 = makes no difference

In Figure 4-4.2, where the resulting data collection is shown, only addresses in the range of 0000 (HEX) to 00FF (HEX) or in the range D000 (HEX) to DFFF (HEX) are collected. (For additional information concerning data qualified clocking, refer to the Clocks and Qualifiers section in the Analyzer's Operator's Manual.)

```
MAIN          TRIG  0063  LXI   SP,E0FFH
              +001  0064      FF     OPERAND FETCH
LOC:  ISIG    +002  0065      E0     OPERAND FETCH
              +003  0066  LXI   H,D000H
SIG:          +004  0067      00     OPERAND FETCH
 098E 0C61    +005  0068      D0     OPERAND FETCH
              +006  0069  LXI   B,1000H
              +007  006A      00     OPERAND FETCH
              +008  006B      10     OPERAND FETCH
              +009  006C  MVI   M,00H
              +010  006D      00     OPERAND FETCH
              +011  D000      00     MEM WRITE
              +012  006E  INX   H
              +013  006F  DCX   B
              +014  0070  MOV   A,B
              +015  0071  ORA   C
```

Figure 4-4.2. Data Qualified Clocking. (Your data may differ.)

4.5 Example 5. Trigger Qualification Using A2.

To use the Model 56 trigger qualification, you need only specify a "1" or "0" for A1 or A2 in the trigger qualifier field of the Analyzer. (See Figure 2-1.) The trigger qualification conditions desired can then be selected using the corresponding A1 and A2 function switches on the Model 56. In Figure 4-5, 250 steps of sequential program operations were collected following a branch step, where the A2 bit was set to a "1" and the A2 switch was set to BRANCH.

STATE ANALYZER MENU (Figure 2-2)	MODEL 56 SWITCHES (Figure 2-1)
Qualifier A1 = X	Switch A1 = makes no difference
Qualifier A2 = 1	Switch A2 = BRANCH

```
MAIN          TRIG   021A  JP     020AH
              +001   021B        0A     OPERAND FETCH
LOC: TRIG     +002   021C        02     OPERAND FETCH
              +003   020A  IN     PORT:E3
SIG:          +004   020B        E3     OPERAND FETCH
 A40E C7EF    +005   E3E3        E8     INPUT
              +006   020C  ANI    08H
              +007   020D        08     OPERAND FETCH
              +008   020E  JZ     --2BH
              +009   020F        2B     OPERAND FETCH
              +010   0211  MOV    A,C
              +011   0212  ANI    DFH
              +012   0213        DF     OPERAND FETCH
              +013   0214  OUT    PORT:E2
              +014   0215        E2     OPERAND FETCH
              +015   E2E2        10     OUTPUT
```

Figure 4-5. Trigger on Branch Operation Using A2 as a Trigger Qualifier. (Your data may differ.) (NOTE: A1 and A2 can be interchanged here.)

5.0 SUMMARY

The powerful clock and triggering capabilities of the Analyzer used in conjunction with the Model 56 (or any of our other dedicated probes) provides you with the highly advanced software-hardware debugging capabilities.

You're encouraged to use Tables 3-1 and 3-2 to expand on the simple examples in this application note. As you use these tables, remember that the A1 and A2 functions can be employed independently, together, or even not at all--when all unqualified collection of address and data is desired. And, since these functions represent **external** qualifier definitions and use status information from the microprocessor itself, the **internal** clock qualification and nested triggering features of the Analyzer are still available and can be used independently to further "select" the data to be collected.

IF YOU HAVE ANY QUESTIONS, SUGGESTIONS OR CRITICISMS, PLEASE FEEL FREE TO CONTACT OUR APPLICATIONS ENGINEERING DEPARTMENT.

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